may transmit a command signal for blocking the clock off sequence to an OR gate in the third full handshake circuit FH3.

[0147] Further, the fourth full handshake circuit FH4 may transmit still another command signal through an OR gate to the third full handshake circuit FH3.

[0148] The third full handshake circuit FH3 blocks the clock off sequence. The third full handshake circuit FH3 may transmit a command signal for blocking the clock off sequence to an OR gate in the second full handshake circuit FH2.

[0149] Further, the third full handshake circuit FH3 may transmit yet another command signal through an OR gate to the second full handshake circuit FH2.

[0150] The second full handshake circuit FH2 blocks the clock off sequence. The second full handshake circuit FH2 may transmit a command signal for blocking the clock off sequence to an OR gate in the first full handshake circuit FH1.

[0151] Further, the second full handshake circuit FH2 may transmit yet another command signal through an OR gate to the first full handshake circuit FH1.

[0152] The first full handshake circuit FH1 blocks the clock off sequence.

[0153] FIG. **7** is a block diagram illustrating an SoC according to at least one example embodiment of the inventive concepts.

[0154] Referring to FIG. **7**, the SoC **500** according to at least one example embodiment of the inventive concepts may include a CMU **510** and at least one IP **520**.

[0155] The CMU **510** may include a first clock source (CK_SC1) **511**, a second clock source (CK_SC2) **512**, a third clock source (CK_SC3) **513**, and a multiplexor **514**. The CMU **510** may provide a clock multiplexor **514** without glitch. A method of outputting a clock without glitch using the SoC **500** is described in FIG. **8** in detail.

[0156] The CK_SC1 **511** generates a first clock CK1. The CK_SC1 **511** transmits the first clock CK1 to the multiplexor **514**.

[0157] The CK_SC2 **512** generates a second clock CK2. The CK_SC2 **512** transmits the second clock CK2 to the multiplexor **514**.

[0158] The CK_SC3 **513** generates a third clock CK3. The CK_SC3 **513** transmits the third clock CK3 to the multiplexor **514**.

[0159] In response to a selection signal SEL, the multiplexor **514** outputs one of the first clock CK1, the second clock CK2, and the third clock CK3. The multiplexor **514** transmits the selected clock to the IP **520**.

[0160] For example, the multiplexor **514** may transmit the first clock CK1 to the IP **520** (Si). Further, the multiplexor **514** may transmit the second clock CK2 to the IP **520** (S2).

[0161] FIG. **8** is a timing diagram illustrating an operation of the SoC shown in FIG. **7**.

[0162] Referring to FIGS. **7** and **8**, the SoC **500** may include a CMU **510** and an IP **520**.

[0163] For example, when a selection signal SEL is changed at time T1, a clock transformed by the multiplexor **514** may output at time T2. Accordingly, from time T1 to time T2, all of the first clock CK1 and the second clock CK2 should be activated.

[0164] Prior to time Ti, the IP **520** activates the first clock request signal REQ1. In response to activation of the clock request signal REQ1, the clock source **511** activates the first clock response signal ACK1. Accordingly, the IP **520** may receive the first clock CK1 through the multiplexor **514** (S1).

[0165] From time Ti to time T2, an output of the multiplexor **514** is transitioned from the first clock CK1 to the second clock CK2. When transitioning from the first clock CK1 to the second clock CK2, a glitch phenomenon may occur.

[0166] To generate a multiplexor clock MUX_CK without a glitch, the first clock source (CK_SC1) **511** generates the first clock CK1 and the second clock source (CK_SC2) **512** generates the second clock CK2 when the first clock CK1 is changed to the second clock CK2 (S2).

[0167] From time T1 to time T2, the first clock request signal REQ1 and the second clock request signal REQ2 are activated. That is, the first clock request signal REQ1 and the second clock request signal REQ2 have a high state.

[0168] Further, the first clock response signal ACK1 and the second clock response signal ACK2 are activated. That is, the first clock response signal ACK1 and the second clock response signal ACK2 have a high state.

[0169] At time T2, the IP **520** receives the second clock CK2 through the multiplexor **514** (S2).

[0170] After time T2, the first clock response signal ACK1 may be deactivated. That is, the first clock response signal ACK1 may have a low state. Accordingly, the first clock CK1 may be deactivated.

[0171] FIG. **9** is a block diagram illustrating at least one example embodiment of a computer system **610** including the SoC shown in FIG. **1**.

[0172] Referring to FIG. **9**, the computer system **610** includes a memory device **611**, an application processor (AP) **612** including a memory controller for controlling the memory device **611**, a radio transceiver **613**, an antenna **614**, a display device **615**, a touch pad **616**, and a touch sensing controller (TSC) **617**.

[0173] The radio transceiver **613** transmits and receives a radio signal through the antenna **614**. For example, the radio transceiver **613** converts the radio signal received through the antenna **614** into a signal to be processed in the AP **612**.

[0174] Accordingly, the AP **612** processes a signal outputted from the radio transceiver **613**, and transmits the processed signal to the display device **616**. Further, the radio transceiver **613** converts the signal outputted from the AP **612** into the radio signal, and transmits the converted radio signal to an external device through the antenna **614**.

[0175] The touch pad **616** may receive a touch signal from a user. The touch pad **616** converts the touch signal into the amount of change of capacitance. The touch pad **616** transmits information about the amount of change of capacitance to the TSC **617**. The TSC **617** converts the information about the amount of change of capacitance into coordinate information. The TSC **617** transmits the coordinate information to the AP **612**.

[0176] In at least one example embodiment of the inventive concepts, the AP **612** may include the SoC **100** shown in FIG. **1**.

[0177] FIG. **10** is a block diagram illustrating another example embodiment of a computer system **620** including the SoC shown in FIG. **1**.

[0178] Referring to FIG. **10**, the computer system **620** may be implemented as a personal computer (PC), a network server, a tablet PC, a netbook, an e-reader, a personal digital assistant (PDA), a portable multimedia player (PMP), an MP3 player, or an MP4 player.